10-Bit, A/D Converter

AD571

1.0 SCOPE

This specification documents the detailed requirements for Analog Devices space qualified die including die qualification as described for Class K in MIL-PRF-38534, Appendix C, Table C-II except as modified herein.

The manufacturing flow described in the STANDARD DIE PRODUCTS PROGRAM brochure at http://www.analog.com/marketSolutions/militaryAerospace/pdf/Die_Broc.pdf is to be considered a part of this specification.

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at www.analog.com/AD571

2.0 Part Number. The complete part number(s) of this specification follow:

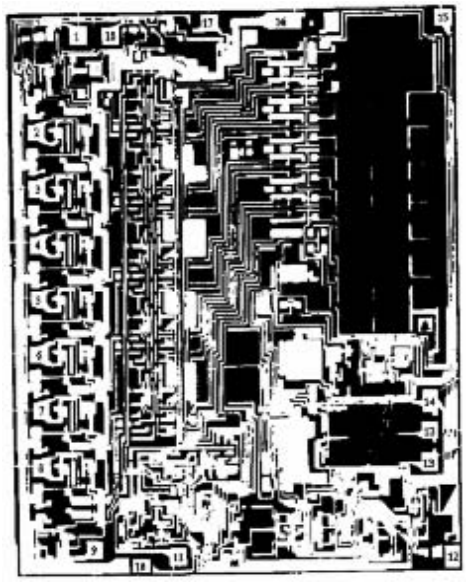
Part Number	Description
AD571-000C	10-Bit, A/D Converter

3.0 Die Information

3.1 Die Dimensions

Die Size	Die Thickness mil	Bond Pad Metalization
126 mil x 158 mil	**19 mil ± 2 mil**	**Al/Cu**

3.2 Die Picture



1. Bit 9
2. Bit 8
3. Bit 7
4. Bit 6
5. Bit 5
6. Bit 4
7. Bit 3
8. Bit 2
9. Bit 1 (MSB)
10. V_{CC}
11. BLK & CONV
12. V_{EE}
13. ANALOG IN
14. ANALOG COM
15. BIPOLAR OFF
16. DIGITAL COM
17. DATA READY
18. BIT 10 (LSB)

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3.3 Absolute Maximum Ratings 1/

Negative Supply Voltage (V_{EE}) to Digital Common.....-16.5V dc
Positive Supply Voltage (V_{CC}) to Digital Common.....+7V dc
Analog Input Voltage to Analog Common.....±15V dc
Digital Input Voltage to Digital Common.....0V dc to V_{CC}
Digital Output Voltage to Digital Common.....0V dc to V_{CC}
Analog Return to Digital Common.....±1V dc
Storage Temperature Range.....-65°C to +150°C
Junction Temperature (T_J).....+175°C
Ambient Operating Temperature Range.....-55°C to +125°C

Absolute Maximum Ratings Notes:

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

4.0 Die Qualification

In accordance with class-K version of MIL-PRF-38534, Appendix C, Table C-II, except as modified herein.
(a) Qual Sample Size and Qual Acceptance Criteria – 25/2
(b) Qual Sample Package – DIP
(c) Pre-screen electrical test over temperature performed post-assembly prior to die qualification.

Table I - Dice Electrical Characteristics

Parameter	Symbol	Conditions 1/	Limit Min	Limit Max	Units
Relative Accuracy	R_A	Unipolar and Bipolar major transitions ±3 codes		±0.195	% FS
Digital Input High Voltage	V_{IH}	BLK and $\overline{CONV}$	2		V
Digital Input Low Voltage	V_{IL}	BLK and $\overline{CONV}$		0.8	V
Digital Input High Current	I_{IH}	BLK and $\overline{CONV}$, V_{IH} = 5V		±100	µA
Digital Input Low Current	I_{IL}	BLK and $\overline{CONV}$, V_{IL} = 0V		±100	µA
Digital Output Low Voltage	V_{OL}	$\overline{DATA}$ $\overline{READY}$, Bit 1 - 10, I_{OL} = +3.2mA		0.4	V
Digital Output High Voltage	V_{OH}	Bit 1 - 10, I_{OH} = -0.5mA	2.4		V
Full Scale Error 2/	A_E	Unipolar		±40	mV
		Bipolar		±20	
Offset Error	V_{OS}	First transition		±0.4	% FS
Bipolar Zero Error	B_{PZE}	Low side MSB, Transition Bipolar		±0.4	% FS

Table I - Dice Electrical Characteristics (Continued)					
Parameter	Symbol	Conditions 1/	Limit Min	Limit Max	Units
Three-State Leakage Current	I_{OLT}	V_{OH} = 5V, V_{OL} = 0V, Bit 1 - 10		±40	µA
Power Supply Current	I_{CC}	BLK and $\overline{CONV}$		10	mA
	I_{EE}		-15		
Differential Nonlinearity 3/	DNL	All codes test Unipolar and Bipolar	10		Bits
Power Supply Rejection	PSRR	-16.0V ≤ V_{EE} ≤ -13.5V V_{CC} = +5V		±78.1	mV
		+4.5V ≤ V_{CC} ≤ +5.5V V_{EE} = -15V			

Table I Notes:

1/ V_{CC} = +5V, V_{EE} = -15V, V_{IH} = +2.0V, V_{IL} = +0.8V, analog input through 15Ω to pin 13, Unipolar configuration. Also, in the Unipolar configuration pin 15 (Bipolar Offset Control) is grounded. T_A = 25°C, unless otherwise specified.

2/ Full Scale Error guaranteed trimmable with 50Ω potentiometer.

3/ Minimum resolution for which no missing codes are guaranteed.

Table II - Electrical Characteristics for Qual Samples

Parameter	Symbol	Conditions 1/	Sub-groups	Limit Min	Limit Max	Units
Relative Accuracy	R_A	Unipolar and Bipolar major transitions ±3 codes	1, 2, 3		±0.195	% of FS
Digital Input High Voltage	V_{IH}	BLK and $\overline{CONV}$	1, 2, 3	2		V
Digital Input Low Voltage	V_{IL}	BLK and $\overline{CONV}$	1, 2, 3		0.8	V
Digital Input High Current	I_{IH}	BLK and $\overline{CONV}$, V_{IH} = 5V	1, 2, 3		±100	µA
Digital Input Low Current	I_{IL}	BLK and $\overline{CONV}$, V_{IL} = 0V	1, 2, 3		±100	µA
Digital Output Low Voltage	V_{OL}	$\overline{DATA}$ $\overline{READY}$, Bit 1 - 10, I_{OL} = +3.2mA	1, 2, 3		0.4	V
Digital Output High Voltage	V_{OH}	Bit 1 - 10, I_{OH} = -0.5mA	1, 2, 3	2.4		V
Full Scale Error 2/	A_E	Unipolar	1		±40	mV
		Bipolar			±20	
Full Scale Temperature Drift	TCA_E		2, 3		±0.488	% FS
Offset Error	V_{OS}	First transition	1		±0.4	% FS
Offset Temperature Drift	TCV_{OS}		2, 3		±0.195	% FS
Bipolar Zero Error	B_{PZE}	Low side MSB, Transition Bipolar	1		±0.4	% FS
Bipolar Zero Temperature	TCB_{PZE}	Bipolar	2, 3		±0.195	% FS
Three-State Leakage Current	I_{OLT}	V_{OH} = 5V, V_{OL} = 0V, Bit 1 - 10	1, 2, 3		±40	µA
Power Supply Current	I_{CC}	BLK and $\overline{CONV}$	1		10	mA
	I_{EE}		1	-15		
Differential Nonlinearity 3/	DNL	All codes test Unipolar and Bipolar	1	10		Bits
Power Supply Rejection	PSRR	-16.0V ≤ V_{EE} ≤ -13.5V, V_{CC} = +5V	1, 2, 3		±78.1	mV
		+4.5V ≤ V_{CC} ≤ +5.5V, V_{EE} = -15V				
Input Resistance	R_{IN}		4	3	7	kΩ
Conversion Time	T_C		9	15	40	µs

Table II Notes:

1/ V_{CC} = +5V, V_{EE} = -15V, V_{IH} = +2.0V, V_{IL} = +0.8V, analog input through 15Ω to pin 13, Unipolar configuration. Also, in the Unipolar configuration pin 15 (Bipolar Offset Control) is grounded.

2/ Full Scale Error guaranteed trimmable with 50Ω potentiometer.

3/ Minimum resolution for which no missing codes are guaranteed.

Table III - Life Test Endpoint and Delta Parameter
(Product is tested in accordance with Table II with the following exceptions)

Parameter	Symbol	Sub-groups	Post Burn In Limit		Post Life Test Limit		Life Test Delta	Units
			Min	Max	Min	Max		
Power Supply Current	I_{CC}	1		10			±1	mA
Digital Output Low Voltage	V_{OL}	1, 2, 3		0.4		0.4	±0.1	V
Digital Output High Voltage	V_{OH}	1, 2, 3	2.4		2.4		±0.24	V
Offset Error	V_{OS}	1		±0.6		±0.8		% FS
Bipolar Zero Error	B_{PZE}	1		±0.6		±0.8		% FS
Unipolar Full Scale Error	A_E UNI	1		±40		±80		mV
Bipolar Full Scale Error	A_E BIP	1		±20		±60		mV

5.0 Life Test/Burn-In Information

5.1 HTRB is not applicable for this drawing.

5.2 Burn-in is per MIL-STD-883 Method 1015 test condition B or C.

5.3 Steady state life test is per MIL-STD-883 Method 1005.

Rev	Description of Change	Date
A	Initiate	Feb. 28, 2002
B	Table III. Change post burn in limits of both Offset Error and Bipolar Zero Error from ±0.2%FS to ±0.6%FS. Update web address.	Sep. 30, 2004
C	Update 1.0 Scope description.	31 July 2007
D	Update header/footer and add to 1.0 Scope description	Feb. 13, 2008
E	Add junction temperature....+175°C to section 3.3-Absolute Maximum Ratings	April 3, 2008
F	Updated Section 4.0c note to indicate pre-screen temp testing being performed	6-JUN-2009